[10191/1294]

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BOARD OF PATENT APPEALS AND INTERFERENCES

Applicants	:	Hartmut BAESSLER et al.
Serial No.	:	09/489,818
Filing Date	:	January 24, 2000
For	:	A METHOD AND A DEVICE FOR CHECKING THE FUNCTIONING OF A COMPUTER
Examiner	:	Marc M. DUNCAN
Art Unit	:	2184
Confirmation No.	:	6309

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Date: 11/20, 2003 Reg. No. 36,197

Signature: _____
Jong H. Lee

APPELLANTS' APPEAL BRIEF
UNDER 37 C.F.R. § 1.192

S I R :

Applicants filed a Notice of Appeal dated August 20, 2003 (filed August 22, 2003) appealing from the Final Office Action dated April 28, 2003, in which claims 1-11 of the above-identified application were finally rejected. This Brief is submitted by Applicants in support of their appeal.

I. REAL PARTY IN INTEREST

The above-identified Applicants and Robert Bosch GmbH of Stuttgart, Germany, are the real parties in interest.

II. RELATED APPEALS AND INTERFERENCES

No appeal or interference which will directly affect, or be directly affected by, or have a bearing on the Board's decision in the pending appeal is known to exist to the undersigned attorney or is believed by the undersigned attorney to be known to exist to Applicants.

III. STATUS OF CLAIMS

Claims 1-11 are pending in this application. Applicants appealed from the rejection of claims 1-11 made in the final Office Action mailed by the Patent Office on April 28, 2003. Of the claims presently on appeal, claims 1 and 8 are independent, and claims 2-7 and 9-11 ultimately depend from claim 1. The claims on appeal are set forth in the Appendix submitted herewith.

IV. STATUS OF AMENDMENTS

No amendment has been filed subsequent to the final Office Action mailed on April 28, 2003.

V. SUMMARY OF THE INVENTION

The present invention provides a method and a device for checking the functioning of a computer, for which purpose an alternate memory and a switchover device are provided. (Abstract). As a result of the switchover device, the access to the computer is diverted such that access is not to the working memory, but rather to the alternate memory. (Abstract). The content of the alternate memory can be influenced by a user, and an auxiliary program may be stored in the alternate memory, which program, when activated by the computer, is executed and makes available information concerning the internal operating states of the computer. (Abstract).

By integrating the analysis program into the normal operating system, it can be assured that important functions can still be monitored by the computer. (P. 1, l. 18-20). Thus, it is assured that even when applications are

running, no disruptions of the essential open-loop or closed-loop control functions of the computer occur as a result of the analysis. (P. 1, l. 20-22).

In Figure 1, a computer (microcontroller) 1 is depicted during the checking of its functioning; microcomputer 1, in a normal operating state, is connected to a working memory 2 via bus lines 5, which are designed both for the exchange of addresses as well as for the exchange of data (address and data bus). (P. 2, l. 5-8). Working memory 2 has a program area 3 and a data area 4; during normal operation, computer 1 processes a program that is contained in the program memory area 3 and for this purpose uses the data that is stored in data area 4. (P. 2, l. 8-11). For the purpose of checking the functioning of computer 1, a changeover switch 6 is provided, which, when activated, connects computer 1 via bus lines 5 to alternate memory 10, and the switch is no longer connected to working memory 2. (P. 2, l. 11-14). Alternate memory 10 has an alternate program area 11, an alternate data area 12, and an auxiliary program area 13. (P. 2, l. 14-15). As indicated by bus lines 50 arranged in Figure 1 to the left of alternate memory 10, alternate memory 10 not only has the capacity to exchange information with computer 1, but it also can be written into or read out from, from the outside. (P. 2, l. 15-18).

Alternatively, it is also possible that changeover switch 6 only changes one part of working memory over to an alternate memory, e.g., it would be possible only to change program area 3 over to alternate program area 11, while data area 4 would be used by computer 1 as before. (P. 2, l. 20-23).

Alternate memory 10 has the property that it can be written into, and the memory content can be read out, from the outside. (P. 2, l. 25-26). This makes it possible to check the mode of functioning of computer 1 and the functioning of selected program parts or data areas. (P. 2, l. 26-27). For this purpose, in alternate memory 10, for example in alternate program area 11 or in alternate data area 12, information is written-in that differs from the

information in program area 3 and in data area 4, respectively. (P. 2, l. 28-30) Computer 1, for example, can be an open-loop control for an internal combustion engine, for which open-loop control tasks, certain closed-loop control programs are stored in the program area, and in data area 4, performance data is stored that is specific to the engine in question and that is used by the closed-loop control programs. (P. 2, l. 31 - p. 3, l. 3). In order to improve the open-loop control of the engine for test purposes, altered closed-loop control programs and altered performance data are written into alternate memory 10, and the check test is thus carried out as to whether the altered closed-loop control or open-loop control programs and the altered performance data bring about an improved functioning of computer 1 or of the functions under the open-loop control of computer 1. (P. 3, l. 3-8). Therefore, in alternate memory 10, an auxiliary program area 13 is provided, in which appropriate auxiliary programs are stored which make possible a checking of the functioning and mode of operation of computer 1 in certain extreme operating states. (P. 3, l. 12-15).

The mode of functioning of this auxiliary program is further explained in connection with Figure 2, which shows alternate memory 10 having alternate program area 11, alternate data area 12, and auxiliary program area 13 is depicted in detail. (P. 3, l. 17-19) Alternate memory 10 is configured, for example, as a so-called dual port RAM, in which, in addition to computer 1, access may be had to alternate memory 10 from the outside. (P. 3, l. 20-22). Auxiliary program 13 contains various areas having various functions: program area 101 is an analysis program, which is executed by computer 1 and which functions to analyze the operating states of computer 1; and an auxiliary program memory area 102 functions to store data for the analysis program. (P. 3, l. 22-26).

Analysis program 101 (i.e., the program that is stored in area 101) is designed to analyze internal states of computer 1, for which purpose analysis

program 101, for example, has the capacity to cause computer 1 to read out the state of individual internal registers, ports, or other memory areas that cannot be read out directly from the outside. (P. 3, l. 28 - p. 4, L. 1). Furthermore, auxiliary program memory area 102 can also be used to communicate to the analysis program which registers, ports, and the like of computer 1 are to be analyzed. (P. 4, l. 6-8). For this purpose, instructions are to be written in from outside into a preselected area of auxiliary program memory area 102, which cause analysis program 101 to investigate the corresponding areas of computer 1. (P. 4, l. 8-11).

For activating auxiliary program 13, provision is to be made for the possibility that computer 1 leaves normal program 11 and is prompted to process auxiliary program 13. (P. 4, l. 13-15). For example, this can occur by making provision in alternate program area 11 for an operating system that from time to time checks to determine whether there is a request from the outside to process auxiliary program 13. (P. 4, l. 15-17). A request of this type could, for example, be written into auxiliary program memory area 102, in which case, the operating system contains a query loop, which checks to determine whether there is a corresponding instruction at the corresponding location of auxiliary program memory area 102. (P. 4, l. 17-21). If a corresponding instruction exists, analysis program 101 is then activated. (P. 4, l. 21).

As depicted in Figure 2, a jump instruction 100 to analysis program 101 may be provided from outside at a predetermined memory location 100 in the normal program flow provided for in alternate program area 11. (P. 4, l. 23-25). This jump instruction, if necessary, is written in from outside into alternate memory 10. (P. 4, l. 25-26). By writing a jump instruction of this type into memory location 100, whenever the program located at the corresponding location in alternate program area 11 is called up, analysis program 101 is processed instead of this program. (P. 4, l. 28-30).

The operating system in alternate program area 11 regularly queries as to whether the activation of analysis program 101 is desired by a user and only permits this to happen if no important control functions have to be monitored by computer 1. (P. 5, l. 26-29). This manner of proceeding also makes it possible to investigate the operating state of computer 1 during the ongoing control function, i.e., under real operating conditions using the real hardware of computer 1, statements can be generated concerning the operating states of computer 1, the execution of a particular program inside computer 1, or concerning the relationship of the internal states of the processor and the closed-loop and open-loop control functions carried out by the computer. (P. 5, l. 29 - p. 6, l. 4).

In the alternative embodiment shown in Figure 3, working memory 2 and alternate memory 10 are only connected to computer 1 by a read line 30, i.e., the programs or data can only be read-out from these memory units. (P. 6, l. 20-22). Furthermore, there is one additional memory chip 41, which is connected to computer 1 both by read line 30 as well as by write line 31, which means the computer 1 can therefore both write as well as read out data in memory 41. (P. 6, l. 22-24). Memory chip 41 is also connected to computer 1 by bus lines 5. (P. 6, l. 24-25).

Memory 41, to which computer 1 has both writing as well as reading access, makes it possible for computer 1 to temporarily store data. (P. 6, l. 28-30). For checking the functioning of computer 1, provision is made for a further memory 42, which is connected to computer 1 by data lines 5 and write line 31. (P. 6, l. 30 - p. 7, l. 1). However, from outside, access can be had to memory 42 that is both writing as well as reading, which access is indicated by bus lines 50 below memory chip 42 in Figure 3. (P. 7, l. 1-2).

Memory chip 42 is arranged by its address area so that its addressable area completely overlaps with the addressable area of memory 41.

(P. 7, l. 4-5). However, provision can additionally be made that memory chip 42 is larger than memory 41 and therefore has an additional addressable area. (P. 7, l. 5-7). By reading out data in memory 42, information concerning the memory content of memory 41 and additional information can also be read out. (P. 7, l. 7-9). Since in every write instruction, as a result of the overlapping address areas, all the data that is written into memory 41 by computer 1 is also simultaneously written into memory 42, by reading out the memory content of memory 42, it can therefore be determined how the memory content of memory 41 looks. (P. 7, l. 9-12).

Furthermore, memory 42 can be used to transport results of analysis program 101 to the outside, for which purpose the analysis program provides that the contents of certain internal registers, ports, etc. of computer 1 are given to the data bus, a write instruction simultaneously being generated and an address being given to the address bus, the address being located in the addressable area of memory 42. (P. 7, l. 14-18). To the extent that no other programs can have access to the corresponding memory locations, this data is also located in an address area in which memory 41 is addressable. (P. 7, l. 18-20). However, if writing this data in memory 41 is to be avoided, for example because memory 41 is entirely needed for the normal operation of computer 1, then the data can be stored in additional address areas of memory 42, in which memory 41 is not addressable. (P. 7, l. 20-23).

VI. ISSUES FOR REVIEW

The following issues are presented for review on appeal in this case:

A) Whether claims 1-8 are anticipated under 35 U.S.C. § 102(b) by U.S. Patent No. 4,212,059 ("Sato").

B) Whether claims 9-11 are unpatentable under 35 U.S.C. § 103(a) over U.S. Patent 4,212,059 ("Sato") in view of U.S. Patent No. 6,105,102 ("Williams").

VII. GROUPING OF CLAIMS

For each ground of rejection in this appeal, all claims subject to the rejection will be argued as one group.

VIII. ARGUMENTS

1. Rejection of Claims 1-8

Claims 1-8 stand rejected under 35 U.S.C. § 102(b) as being anticipated by United States Patent No. 4,212,059 to Sato et al. ("Sato"). It is respectfully submitted that the rejection of claims 1-8 as being anticipated by the Sato reference should be reversed for at least the following reasons.

To reject a claim under 35 U.S.C. § 102(b), the Office must demonstrate the presence in a single prior art reference disclosure of each and every element of the claim invention, *arranged as in the claim.* See Lindeman Machinenfabrik v. American Hoist and Derrick, 730 F.2d 1452, 1458 (Fed. Cir. 1984). "The identical invention must be shown in as complete detail as is contained in the claim." M.P.E.P. § 2131. If any claimed element is absent from a prior art reference, it cannot anticipate the claim. See Rowe v. Dror, 112 F.3d 473, 478 (Fed. Cir. 1997).

Independent Claim 1 recites:

> A method for checking a functioning of a computer, the computer, **in a normal operating state, accessing a working memory using bus lines**, a content of the working memory being able to be influenced by a user, the method comprising the steps of:
>
> **diverting an access of the computer, by a switchover device, such that the access is directed to an alternate memory rather than to the working memory**; and
>
> executing an auxiliary program in the alternate memory when activated by the computer, the auxiliary program making available information concerning internal

operating states of the computer. (*emphasis added*).

Thus, according to Claim 1, computer access to the working memory is **diverted** to an alternate memory, and **the auxiliary program in the alternate memory** is executed; the auxiliary program is not executed in the working memory. The Sato reference clearly fails to disclose two separate limitations: 1) diverting an access of the computer from a working memory to an alternate memory; and 2) executing an auxiliary program in the alternate memory. However, in response to Applicants' arguments contained in the Amendment mailed on April 9, 2003, the Examiner made the following arguments in the final rejection mailed on April 28, 2003:

> Applicants argue that the Sato reference does not teach, "executing an auxiliary program in the alternate memory." Applicants argue that Sato in fact teaches executing the auxiliary program in same memory as the normal processing routine. The examiner respectfully disagrees. The examiner **believes** that the actual execution of the program must take place in the processor, i.e. the processor retrieves the instructions of the program from the memory and then executes them. **The examiner therefore believes that the Sato reference teaches the processor taking the instructions for the "abnormal processing routine" from the alternate memory (the flexible disk unit of Sato), transferring these instructs to an area in the processor and executing them.** The examiner believes that this is equivalent in function to applicants' claimed invention. The examiner **believes** applicants' claimed invention switches to the claimed alternate memory, takes the program instructions from the alternate memory area and executing the instructions in the processor. The examiner therefore maintains the rejection of claim 1 using the previously provided reference to Sato. (Office Action, p. 5, l. 10 – p. 6, l. 2). (*emphasis added*).

The Sato reference discloses the following: (1) the operation console is comprised of an operation processor, a flexible disk storage unit, a CRT display, and a keyboard (Sato, col. 3, ll. 24 – 26); (2) the operation processor comprises a microprocessor 300 and memories 301-303 (Sato, col. 3, ll. 26 – 27); (3) the flexible disk stores both the abnormal and normal processing

routines (Sato, col. 9, ll. 53 – 58); (4) for execution, the abnormal processing routine is read out from the flexible disk onto the overlay area for execution (Sato, col. 9, ll. 44 – 49). Thus, in Sato, **both the normal and abnormal routines are stored on the flexible disk, and the execution of both routines occurs in processor memories 301-303**.

As applied to the limitations of Claim 1, memories 301 – 303 of Sato are the working memory for the processor, and, as asserted by the Examiner, the flexible disk may be the alternate memory. Under this interpretation, the Sato reference clearly does not disclose: 1) **diverting access** from the working memories 301-303, or any part thereof, to the alternate memory; and 2) then executing an auxiliary program in the alternate memory. Indeed, the Examiner acknowledges that the processor executes both programs (normal and abnormal) in the processor's working memory (memories 301-303). However, because the Examiner "**believes** that the actual execution of the program must take place in the processor," the Examiner states that he "**believes** applicants' claimed invention switches to the claimed alternate memory, takes the program instructions from the alternate memory area and executing the instructions in the processor," and that he "**believes** that [Sato's method] is equivalent in function to applicants' claimed invention." (4/28/03 Office Action, p. 5-6). **Essentially, the Examiner's argument appears to be as follows: 1) "the actual execution of the program must take place in the processor"; 2) Sato retrieves an auxiliary program from an alternate memory and transfers the program to an area in the processor for execution; 3) Applicants invention must involve transferring the auxiliary program from the alternate memory to the processor and executing the auxiliary program in the processor; and 4) therefore, Sato teaches Applicants' claimed invention.** The Examiner's argument is fundamentally flawed, as explained below in detail.

First, it is quite irrelevant what the Examiner **believes** the invention should be; instead, one must look to the claim language to determine the

invention sought to be claimed. In this regard, the Examiner is not only ignoring, but actually changing, the limitations of Applicants' Claim 1 regarding "diverting an access of the computer, by a switchover device, such that the access is directed to an alternate memory rather than to the working memory." While the Examiner argues that merely fetching the "abnormal processing routine" from the alternate memory and executing this routine in the processor memory (according to the Examiner's interpretation of Sato) satisfies the Applicants' claimed limitation of "diverting an access of the computer, by a switchover device, such that the access is directed to an alternate memory rather than to the working memory," there is no indication in Sato that an **access of the computer is diverted by a switchover device** from the working memory 301-303 to an alternate memory (floppy disk). In fact, the Examiner's own argument leads to the conclusion that the access to the working memory 301-303 must be intact in Sato in order to complete the transferring of the abnormal processing routine to the working memory 301-303.

Regarding the limitation "executing an auxiliary program in the alternate memory," to the extent the Examiner is applying the **doctrine of equivalents** to argue that Sato discloses the above-recited limitation, the Examiner's argument violates the Supreme Court's guidance that "the application of the doctrine, even as to an individual element, is not allowed such broad play as to **effectively eliminate that element in its entirety**." Sato clearly does not teach "executing an auxiliary program in the alternate memory." Indeed, the Examiner does not dispute this; instead, the Examiner merely argues that the auxiliary program must be executed in the processor, i.e., the program to be executed must be at least temporarily stored in the memory associated with the processor, e.g., memory 301-303 in Sato. However, this assertion by the Examiner is not only contrary to the plain language of Claim 1, but also based on incorrect assumptions regarding the present invention. There is no indication in Applicants' disclosure or the claim language that the alternate memory recited in Claim 1 may not be a memory associated

with the processor.

For the foregoing reasons, Sato fails to disclose diverting, by a switchover device, the access of the computer from the working memory to the alternate memory, and executing the auxiliary program in the alternate memory. Since Sato does not disclose each and every feature of Claim 1, Sato does not anticipate Claim 1 or its dependent Claims 2-7.

Claim 8 recites "means for redirecting a connection of the computer from a working memory to the alternate memory," similar to the limitation recited in Claim 1, i.e., "diverting an access of the computer, by a switchover device, such that the access is directed to an alternate memory rather than to the working memory." Accordingly, for the reasons stated in connection with Claim 1, Applicants submit that Sato does not anticipate Claim 8.

It is respectfully requested that the rejection of Claims 1-8 as being anticipated by Sato be reversed.

B. Rejection of Claims 9-11

Claims 9-11 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the Sato reference in view of United States Patent No. 6,105,102 to Williams et. al. ("Williams"). It is respectfully submitted that the obviousness rejection of claims 9-11 as being unpatentable over the combination of Sato and Williams should be reversed for at least the following reasons.

To establish a prima facie case of obviousness, three criteria must be satisfied. First, there must be some suggestion or motivation to modify or combine reference teachings. In re Fine, 837 F.2d 1071, 5 U.S.P.Q.2d 1596 (Fed. Cir. 1988). This teaching or suggestion to make the claimed combination must be found in the prior art and not based on the application disclosure. In

re Vaeck, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Second, there must be a reasonable expectation of success. In re Merck & Co., Inc., 800 F.2d 1091, 231 U.S.P.Q. 375 (Fed. Cir. 1986). Third, the prior art reference(s) must teach or suggest all of the claim limitations. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974).

"All words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424F.2d 1382, 1385, 165 U.S.P.Q. 494, 496 (C.C.P.A. 1970). Furthermore, a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. See W.L. Gore & Associates, Inc. v. Garlock, Inc., 721 F.2d 1540, 220 U.S.P.Q. 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984); see also, Akzo N.V. v. United States Int'l Trade Comm'n, 1 U.S.P.Q.2d 1241, 1246 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987)(it is impermissible to pick and choose among individual parts of assorted prior art references as a mosaic to recreate a facsimile of the claimed invention).

In addition to the above, generalized assertions that it would have been obvious to modify the reference teachings do not properly support a § 103 rejection. See In re Fine, supra; In re Jones, 21 U.S.P.Q.2d 1941 (Fed. Cir. 1992). As noted by the Court in the case of In re Fine, "a *prima facie* case of obviousness . . . [can be established] only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references." In re Fine, 5 U.S.P.Q.2d at 1598 to 1600.

Claims 9-11 depend from Claim 1. As discussed above in connection with Claim 1, the Sato reference fails to disclose "diverting an access of the computer, by a switchover device, such that the access is directed to an alternate memory rather than to the working memory." The Williams reference similarly fails to teach or suggest this limitation. Since the Sato and Williams

references fail to disclose each and every feature of Claim 1, the Sato and Williams references do not render dependent Claims 9-11 obvious under 35 U.S.C. §103(a).

Independent of the above, Applicants note that the asserted combination of Sato and Williams fails to achieve the claimed invention of claim 9 for additional reasons, and that there is no motivation for making the asserted combination. While the Examiner states that "Williams teaches a step of performing a check periodically to determine whether there is a request from an outside source to process the auxiliary program in the Abstract, lines 7-10," there is simply no teaching or suggestion in Williams that the polling is to determine "whether there is a request from an outside source to process the auxiliary program" as asserted by the Examiner. In fact, Williams describes that a peripheral device 102 issues an interrupt to the CPU 108 to indicate that **an information frame received from the communications network 106 needs processing** by the CPU. (Col. 1, l. 54-58). This has nothing to do with "whether there is a request from an outside source to process the auxiliary program" as asserted by the Examiner.

Furthermore, while the Examiner contends that one of ordinary skill in the art would have been motivated to combine Sato and Williams because "the host system will avoid processing resources needed for context switching time when the subsequent interrupt, or request, is generated closely in time from the prior interrupt," Applicants note that Williams explicitly teaches that the "host system operates in a polling mode **if the predicted [future] interrupt time point is before a predetermined time period after the end of the prior interrupt service routine**," and the "host system operates in an interrupt mode [non-polling mode] if the predicted [future] interrupt time point is after the predetermined time period after the end of the prior interrupt service routine." (Abstract). Given the fact that the decision to enter into the polling mode in Williams is dependent on the initial prediction regarding when

the future interrupt will occur, it is simply conclusory assertion of a hindsight reconstruction to argue that one of ordinary skill in the art would selectively pick the polling mode and apply it to the teachings of Sato, which does not teach a step of performing a period check, let alone teach anything about predicting when the future interrupt will occur.

For the foregoing reasons, claim 9 and its dependent claims 10-11 are not rendered obvious by the asserted combination of Sato and Williams. It is therefore respectfully requested that this rejection be reversed.

IX. CONCLUSION

For the foregoing reasons, it is respectfully submitted that the final rejection of claims 1-11 should be reversed.

Respectfully submitted,

KENYON & KENYON

Dated: 11/20, 2003

By: for Richard L. Mayer (by [signature])
Richard L. Mayer
Reg. No. 22,490

R. No. 36,197)

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[10191/1294]

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Date: 11/20, 2003 Reg. No. 36,197

Signature: _____
Jong H. Lee

APPENDIX TO APPELLANTS' APPEAL BRIEF
UNDER 37 C.F.R. § 1.192

S I R :

The claims involved in this appeal, claims 1-11, in their current form after entry of all amendments presented during the course of prosecution, are set forth below:

APPEALED CLAIMS:

1. A method for checking a functioning of a computer, the computer, in a normal operating state, accessing a working memory using bus lines, a content of the working memory being able to be influenced by a user, the method comprising the steps of:

diverting an access of the computer, by a switchover device, such that the access is directed to an alternate memory rather than to the working memory; and

executing an auxiliary program in the alternate memory when activated by the computer, the auxiliary program making available information concerning internal operating states of the computer.

2. The method according to Claim 1, further comprising the step of posing instructions in the auxiliary program as to which information regarding the computer should be investigated.

3. The method according to claim 1, wherein the auxiliary program contains program steps that cause the computer to give a content of internal registers and ports to a bus using a write instruction for a certain address.

4. The method according to claim 3, further comprising the step of reading out, by the user, a memory in an address area.

5. The method according to claim 1, further comprising the step of executing

an instruction in an alternate program area for causing the computer to begin processing an analysis program and for activating the auxiliary program.

6. The method according to claim 5, wherein the alternate program memory contains a first program module and a second program module of greater importance than the first program module, and further comprising the step of writing the instruction into the first program module.

7. The method according to claim 1, further comprising the steps of:

using an operating system, generating a query as to whether an analysis of the computer should be undertaken; and

using the operating system, activating an analysis program if the query is answered affirmatively.

8. A device for checking a functioning of a computer, comprising:

a readable alternate memory including an auxiliary memory area, the auxiliary memory area containing an analysis program, the analysis program, when activated, supplying information concerning internal states of the computer; and

means for redirecting a connection of the computer from a working memory to the alternate memory.

9. The method according to Claim 1, further comprising the step of performing a check periodically to determine whether there is a request from an outside source to process the auxiliary program.

10. The method according to Claim 9, further comprising the step of executing an analysis program in response to determining that the request has been provided.

11. The method according to Claim 9, wherein one of a jump instruction and an interrupt instruction is provided at a predetermined memory location to start processing an analysis program.

Respectfully submitted,

KENYON & KENYON

Dated: 11/20, 2003

By: [signature]
Richard L. Mayer
Reg. No. 22,490
(Reg. No. 30,197)

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